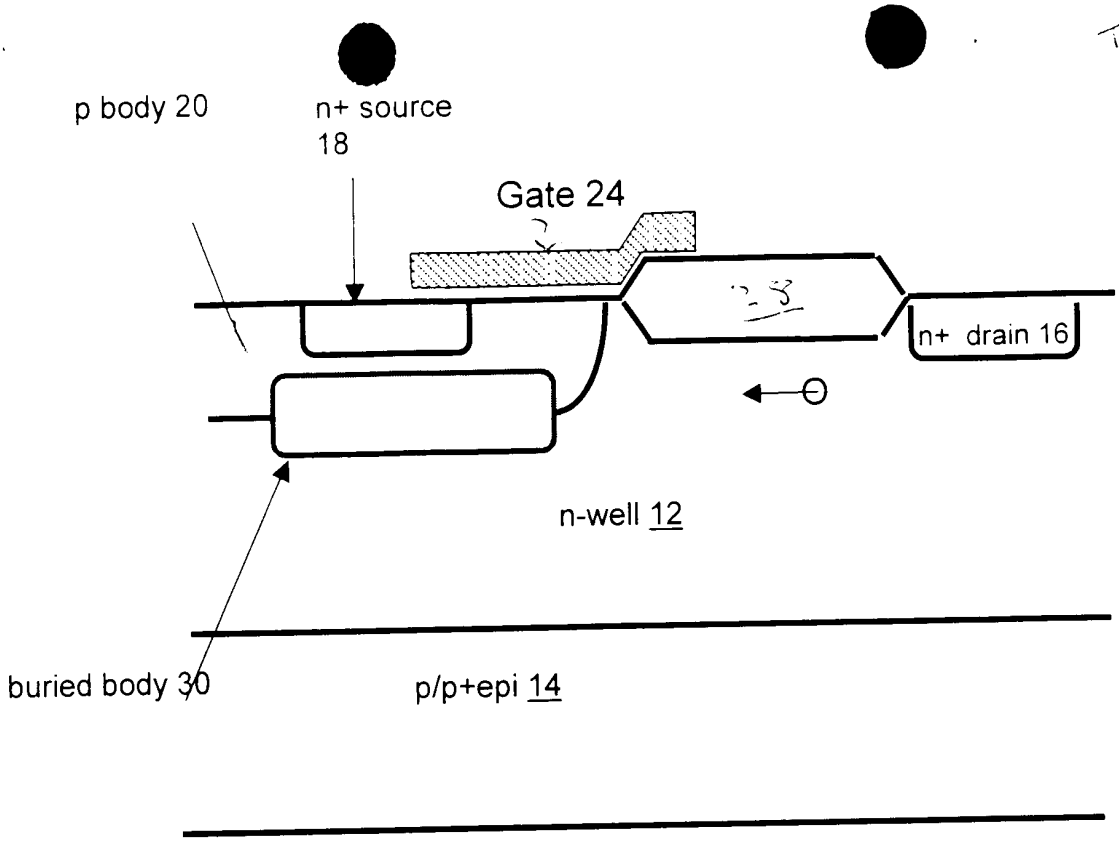

p body 20
n+ source
18
Gate 24
n+ drain 16
n-well 12
buried body 30
p/p+epi 14

Figure 1

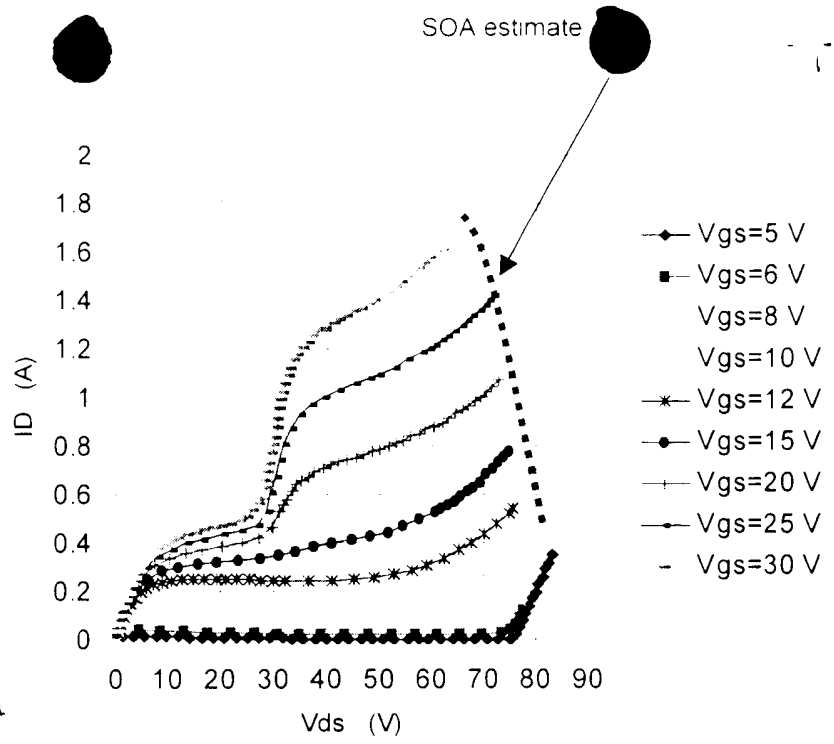


Fig. 2R. Drain characteristic for buried body LDMOS. Pulse measurements with pulse time of 100ns. The approximate location of the SOA boundary is indicated by the dashed line. The increase in ID seen near Vds=30V is an indication that charge compensation due to holes is occurring in the Nwell. W=0.0938 cm.

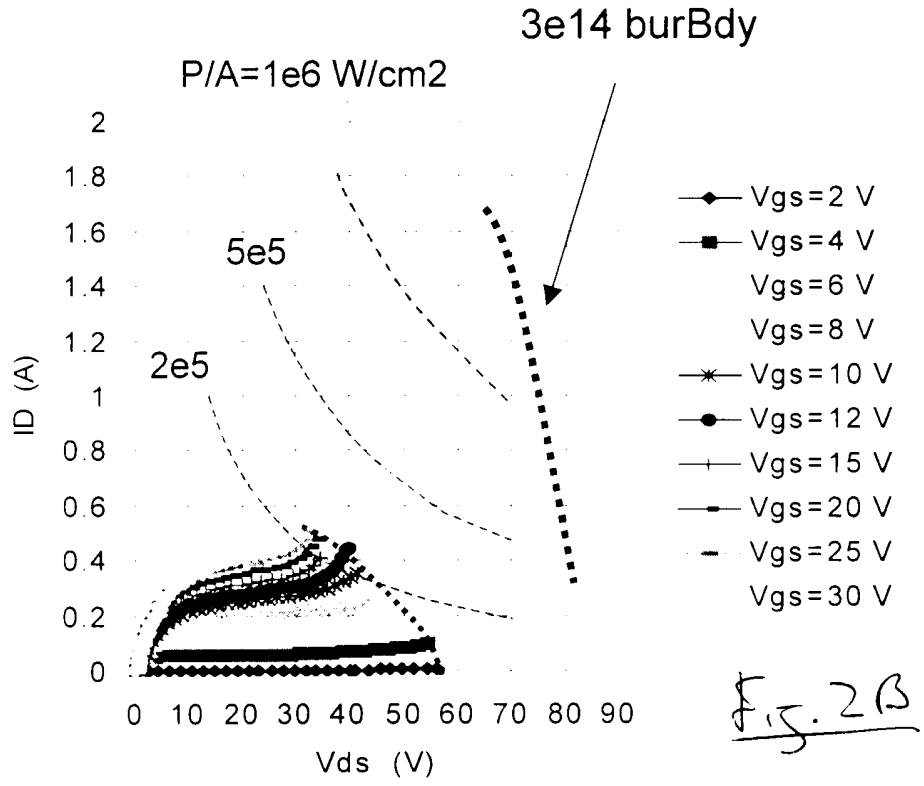
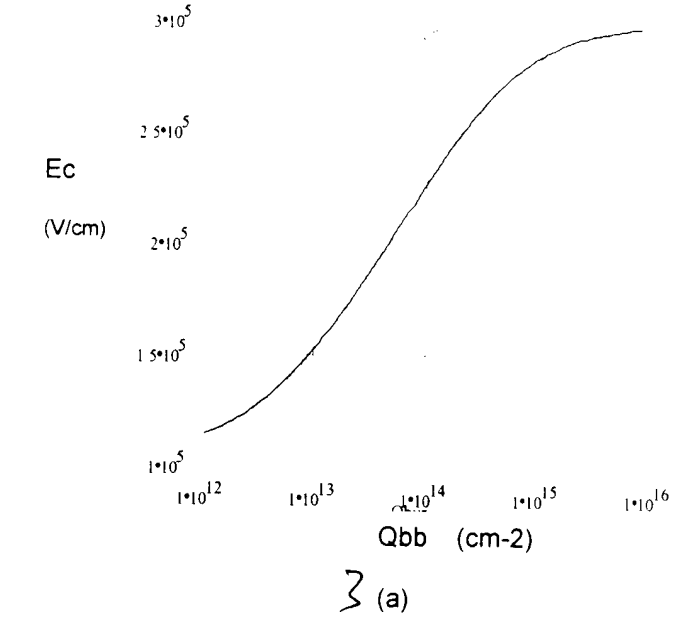
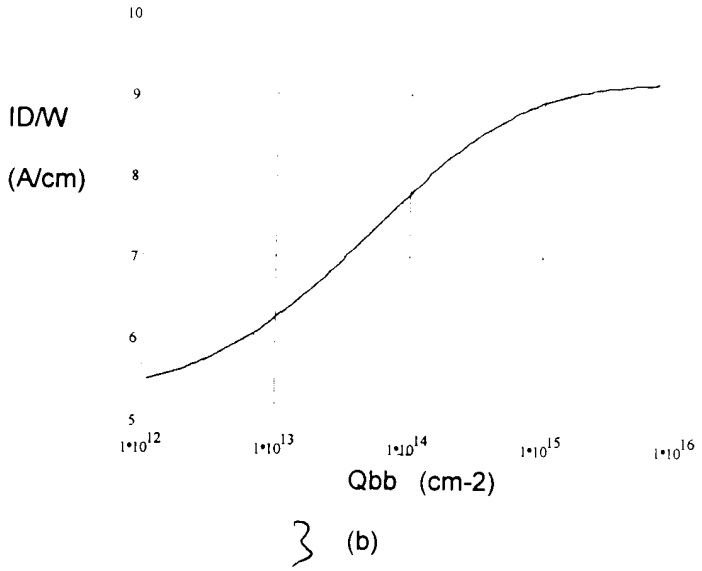


Fig. 3. Drain characteristic for the same LDMOS as in Fig. 2R but without the buried body. The SOA for the buried body LDMOS is indicated and exceeds 1e6 W/cm2 and shows more than a factor of 5 improvement over the conventional LDMOS.



(a)



(b)

Fig. 3. (a) critical field vs. buried body dose for an n-Ldmos constructed as in Fig. 1. Calculating using the one-dimensional model of [1] and Eqs. (2), (3), and (4). (b) Corresponding drain current per unit gate width vs. buried body dose.

Done prior to this step

Material Start, 20um p-epi on p+ sub <100>
First oxidation 7500A
Hard mask deposit
n+ buried layer photo and etch
Antimony implant 3 to 6e15 cm-2
Buried layer diffusion*
Strip surface oxide
p-epi deposit 9 to 10 um 7ohm-cm
2nd oxidation 7500A

*not shown here, for a "low-side" Ldmos. A "high-side" Ldmos will have an n+ buried layer placed beneath the window.

This step

Nwell photo
oxide etch
Nwell implant phosphorous 3 to 5 e12 cm-2

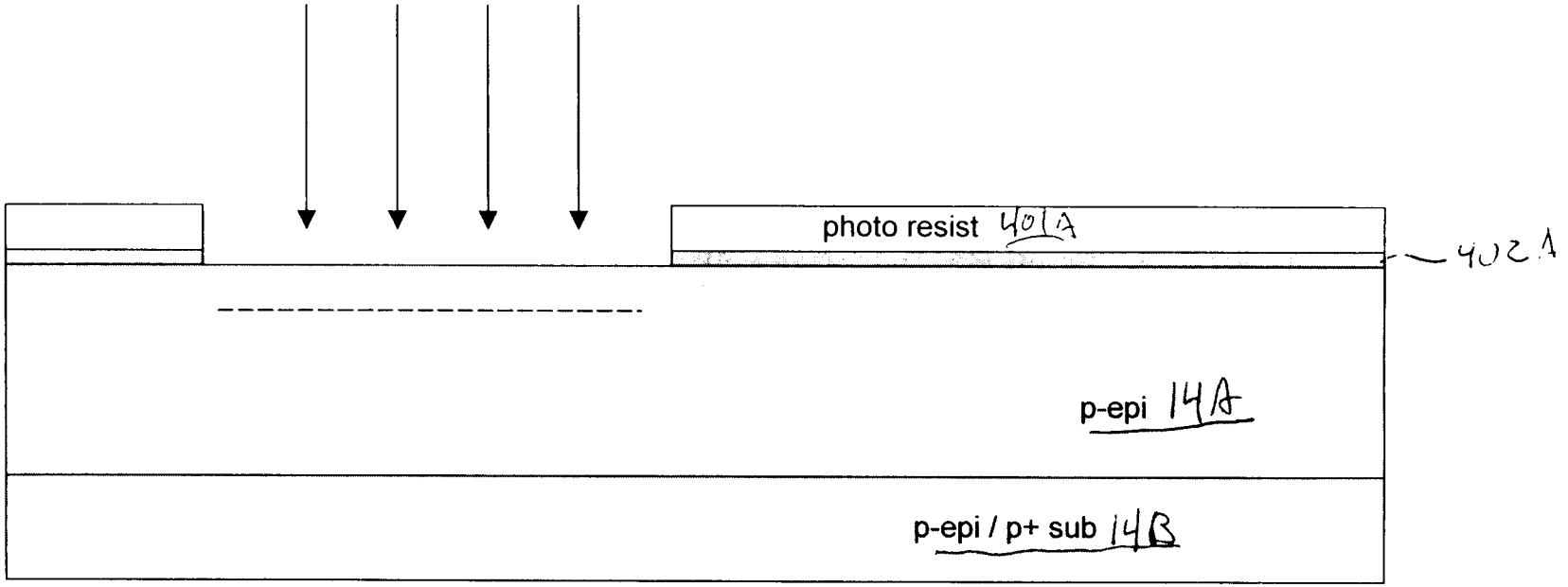


Fig. 4A

Done prior to this step

Nwell diffusion xj= 4 to 6 µm
n+sinker photo and etch
n+ deposit POCl3
strip oxide
pad oxidation 350A
CMOS Nwell photo and implant (not shown)
CMOS Pwell photo and implant (not shown)
diffusion

This step

Dwell (p-body) photo
Dwell Boron implant 3 to 7e13 @ 50 keV
Dwell Arsenic implant 3 to 8 e13 @ 135 keV
Dwell Boron MeV implant 1 to 4e14 @ 300 to 600 keV
(Buried Body)

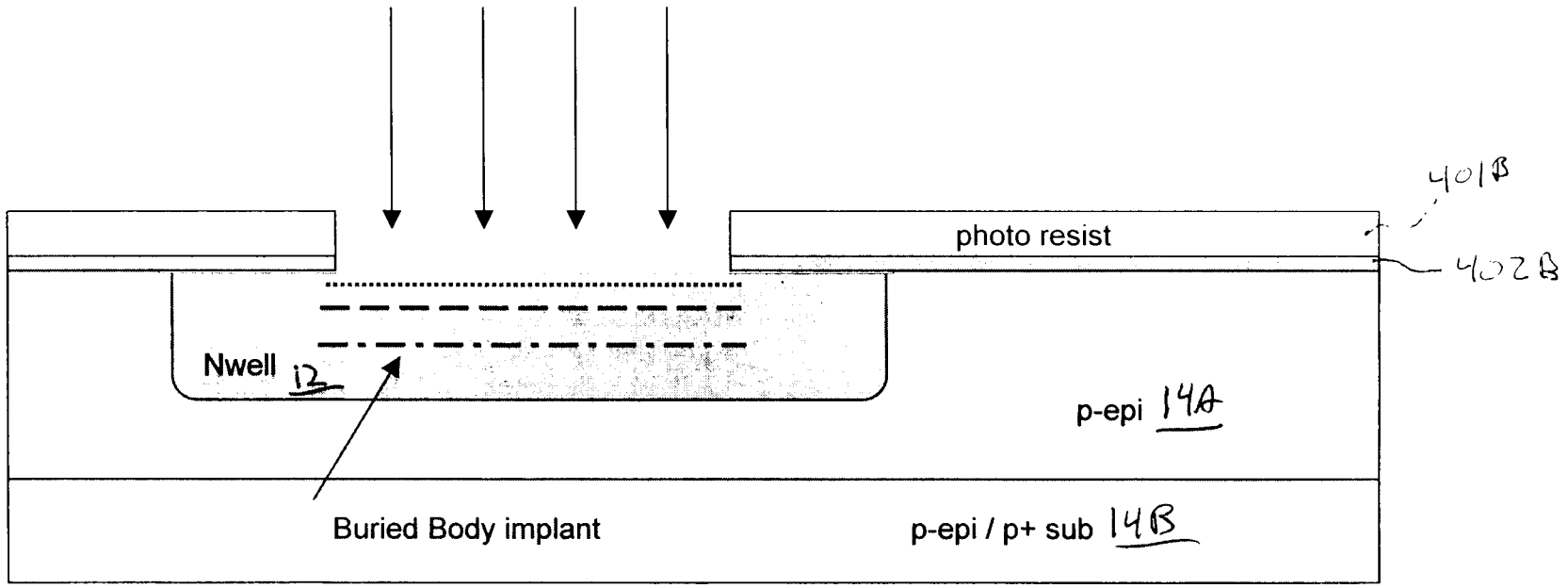


Fig. 4B

Done prior to this step

Dwell diffusion xj– 2 to 2.5 μm
strip oxide
pad oxidation 200 to 400A
Base photo (not shown)
Base implant (not shown)
nitride deposition 1000 to 1500A
Locos photo and nitride etch
resist strip

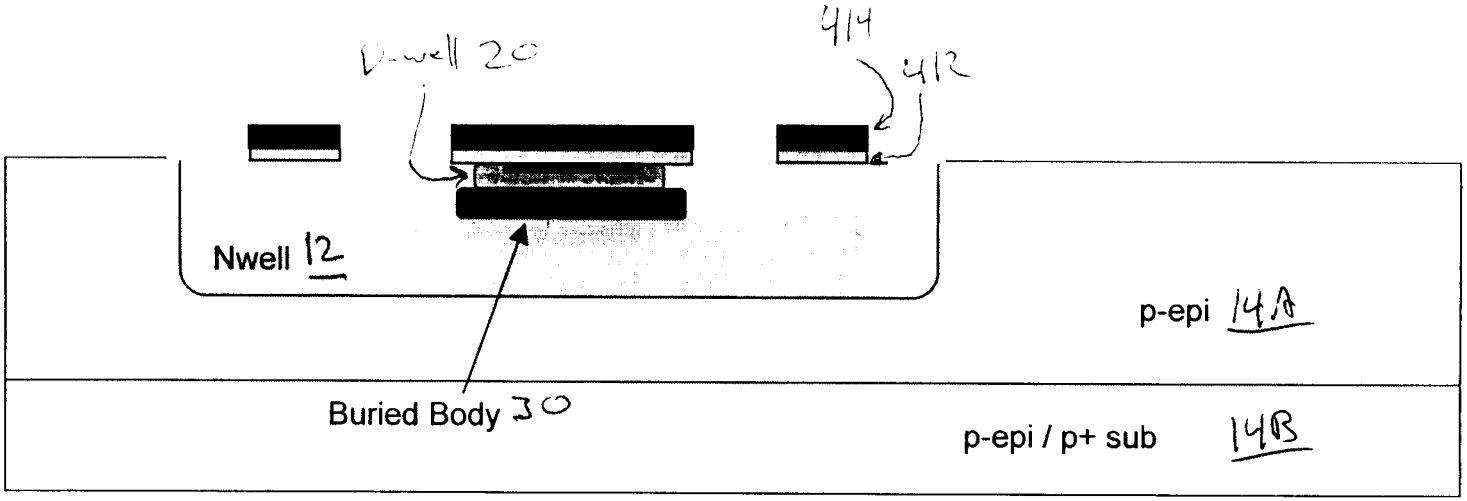


Fig. 4C

Done this step

Field oxidation 6000 to 7000 A

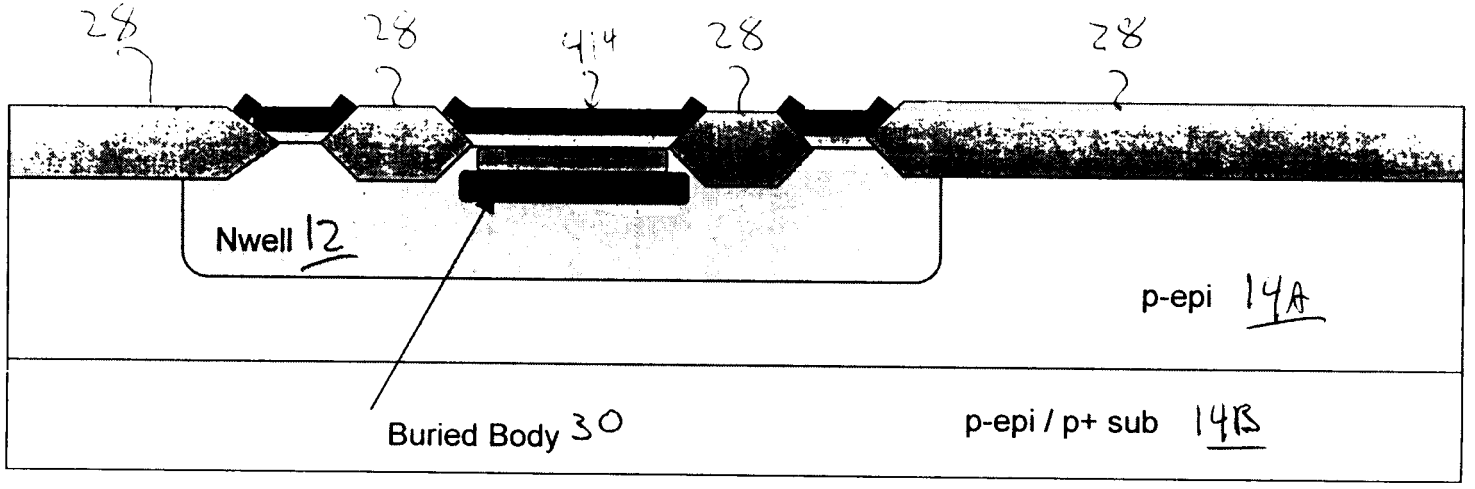


Fig. 4D

Done prior to this step

strip nitride
sacrificial oxidation 300A
etch oxide 800 A
gate oxidation 300 to 400 A
threshold adjust photo and implants (not shown)

Done this step

SNwell photo

SNwell MeV implant Phos 3 to 6 e13 @ 800 to 900 keV

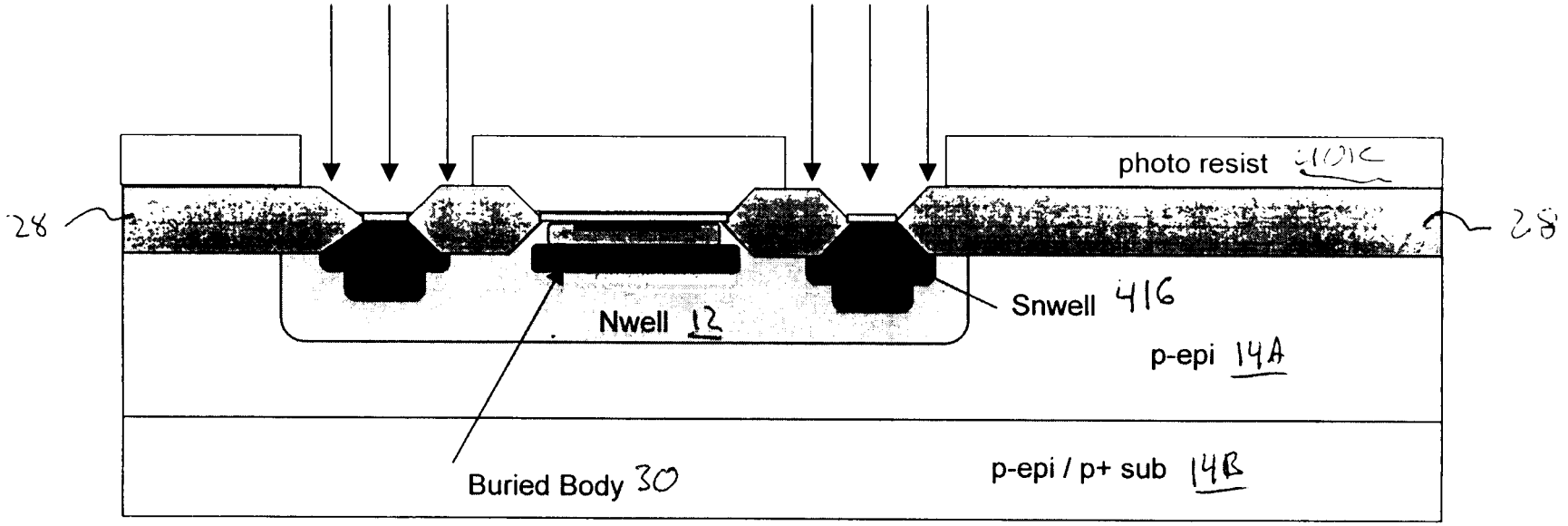


Fig. 4E

Done prior to this step
Strip photo
SNwell Rapid Thermal Anneal
Deposit n+ poly 5kA
poly photo and etch
cap oxide deposit 350A TEOS
CMOS nLDD and pLDD photo and implants (not shown)
nitride sidewall deposit 1200 to 1600 A
nitride sidewall etch

This step
n+ source/drain photo n+ source/drain implant Phosphorous 2 to 6e14 cm-2 n+ source/drain implant Arsenic 2 to 4e15 cm-2 strip resist

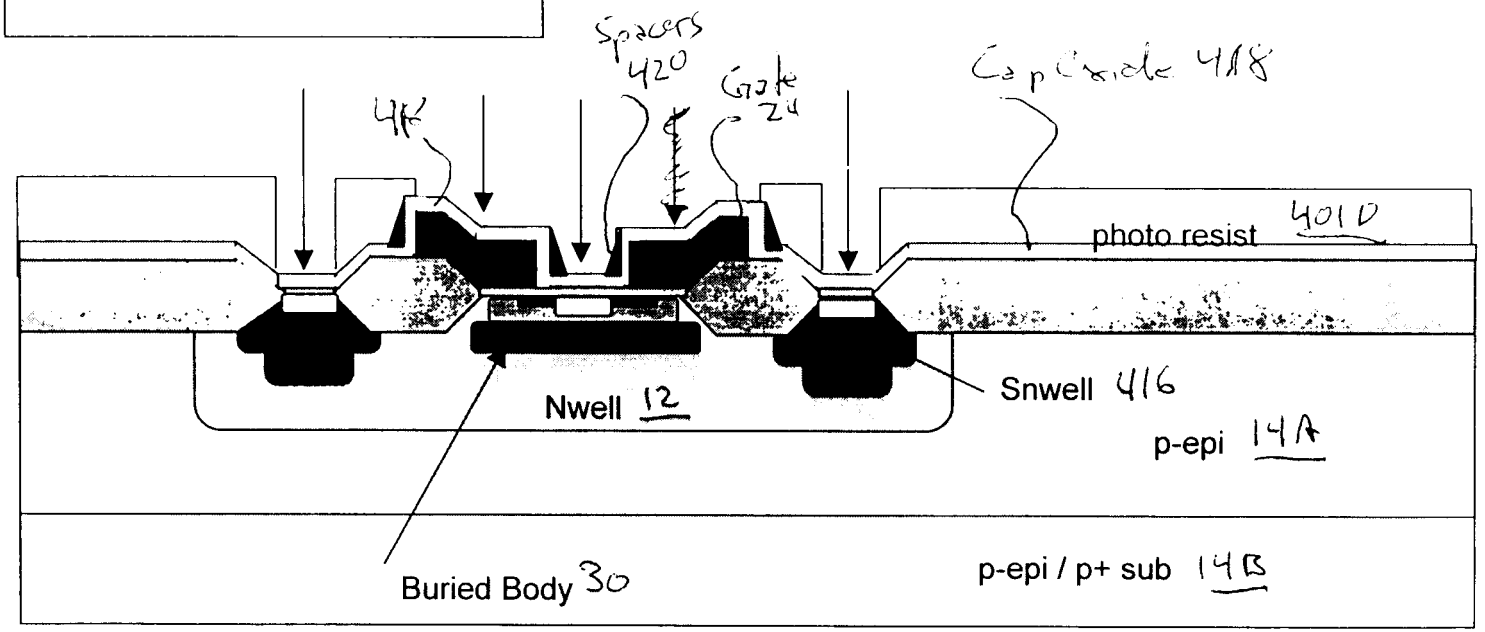


Fig. 4F

Done this step

p+ source/drain photo
p+ source/drain implant Boron 1.5 to 3e15
strip resist

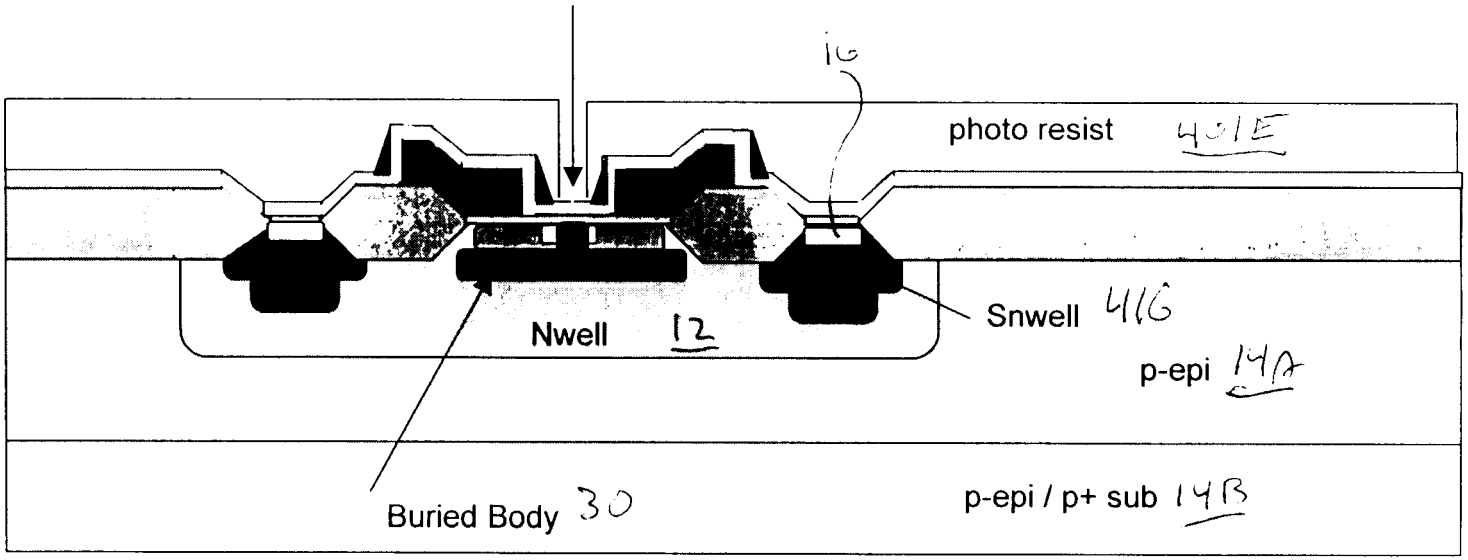


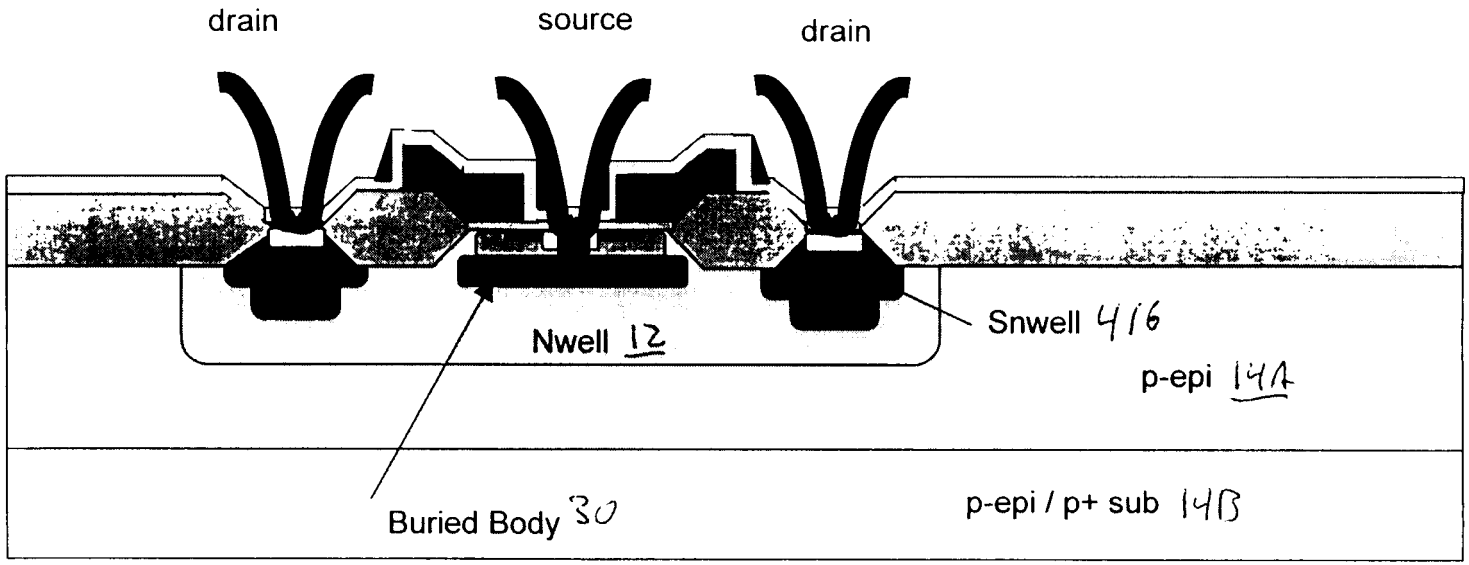
Fig 4/6

Done prior to this step

Deposit NSG (non-doped silicon glass) plus
BPSG (boron and phosphorous doped silicon glass)
6kA to 9kA (not shown)
BPSG densification (will flow glass, rounding sharp edges)
Contact photo and etch
Platinum deposit 300 to 600 A
Platinum sinter
Aqua regia etch (removes Pt on oxide and leaves Platinum silicide in contact areas)

Done this step

Deposit Metal Al/Si/TiW 5k to 8k A
Metal photo
Metal etch (metal pattern will conform to curved BPSG layer, needed for step coverage)



Lbc5 60V Low-side Ldmos

nch_ldmls_hv3

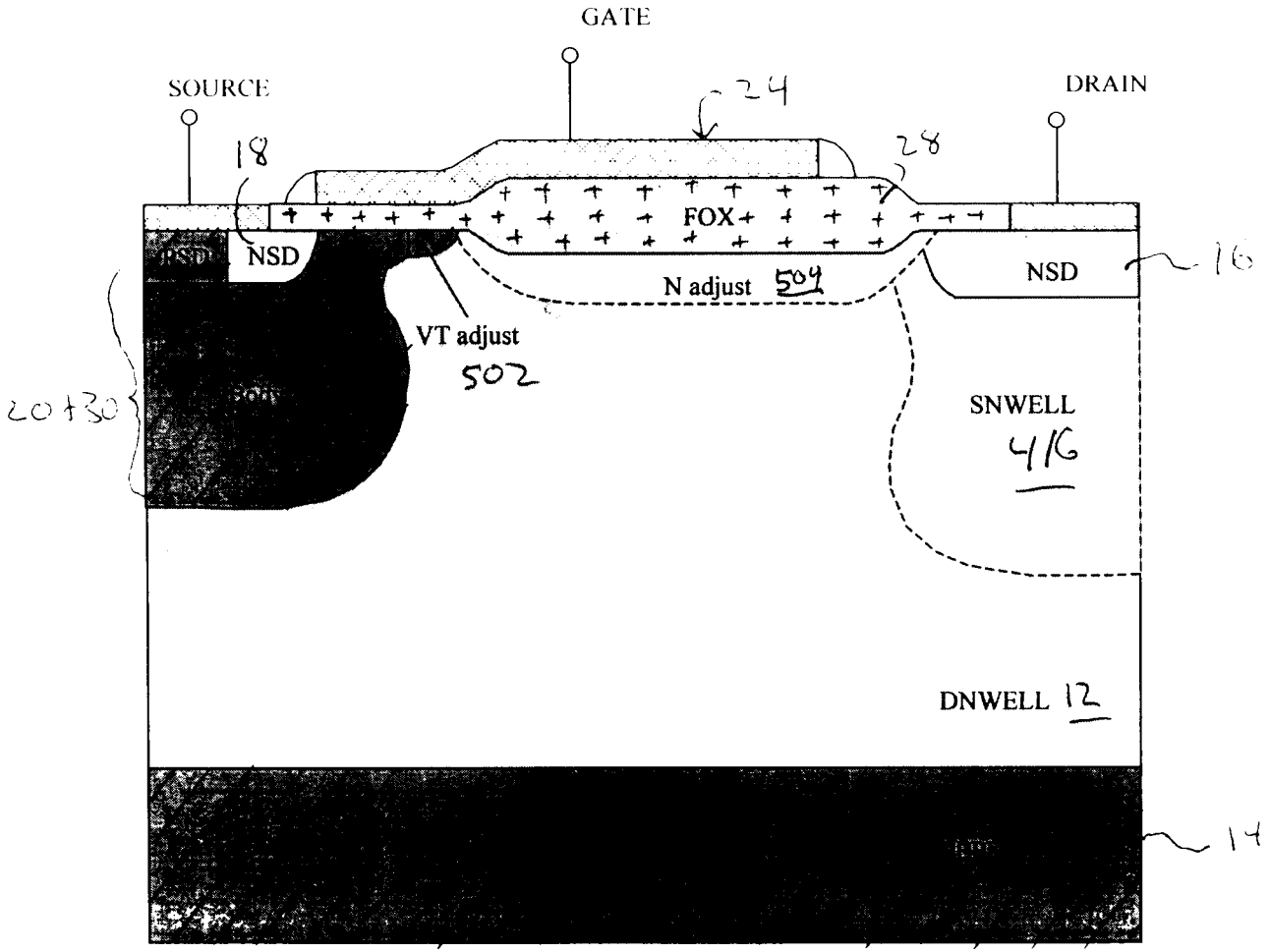


Fig. 5A

Lbc5 50V High-side Ldmos
nch_ldmhs_hv2

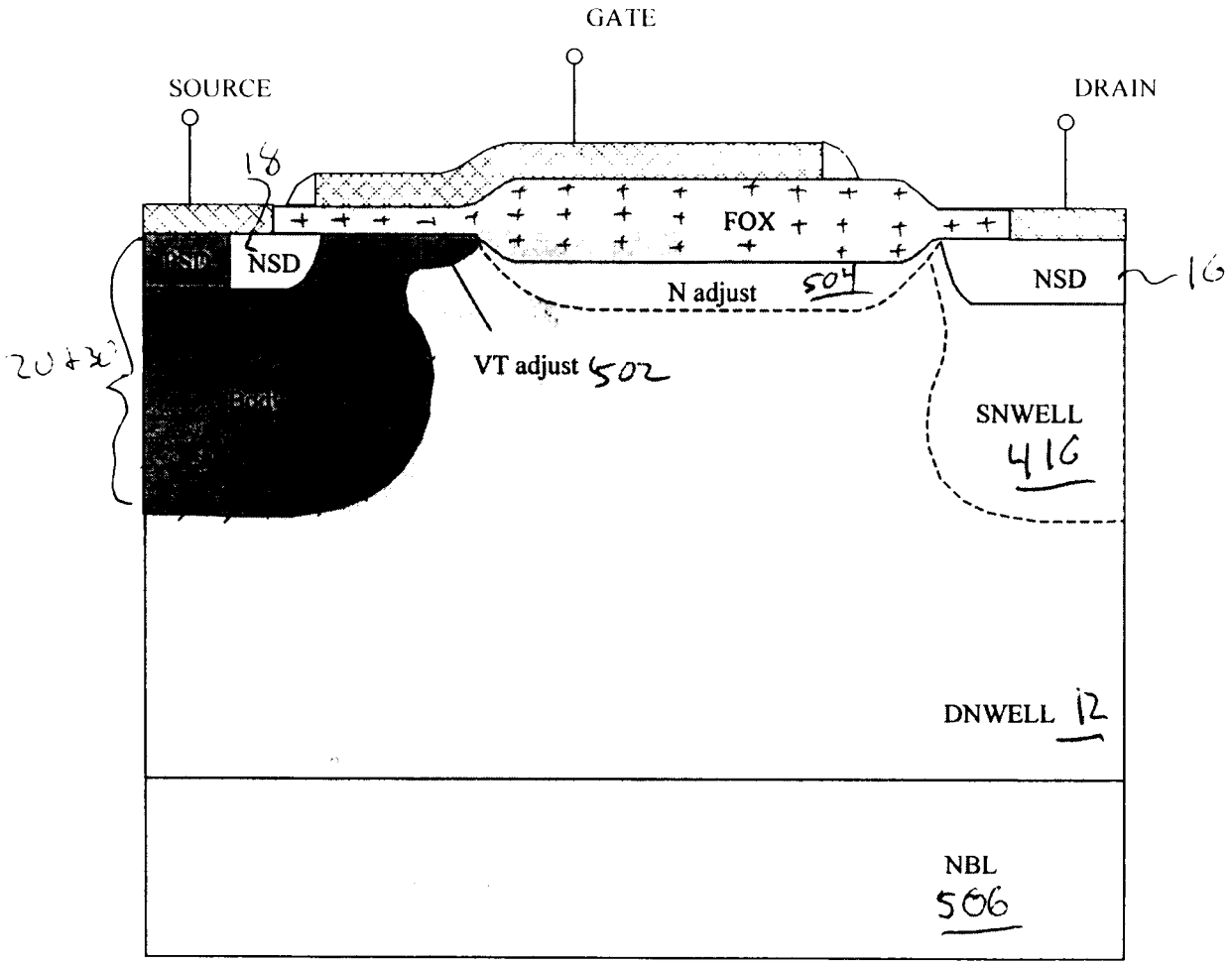


Fig 5B

Lbc5 25V Low-side Ldmos
nch_ldmls_mv2

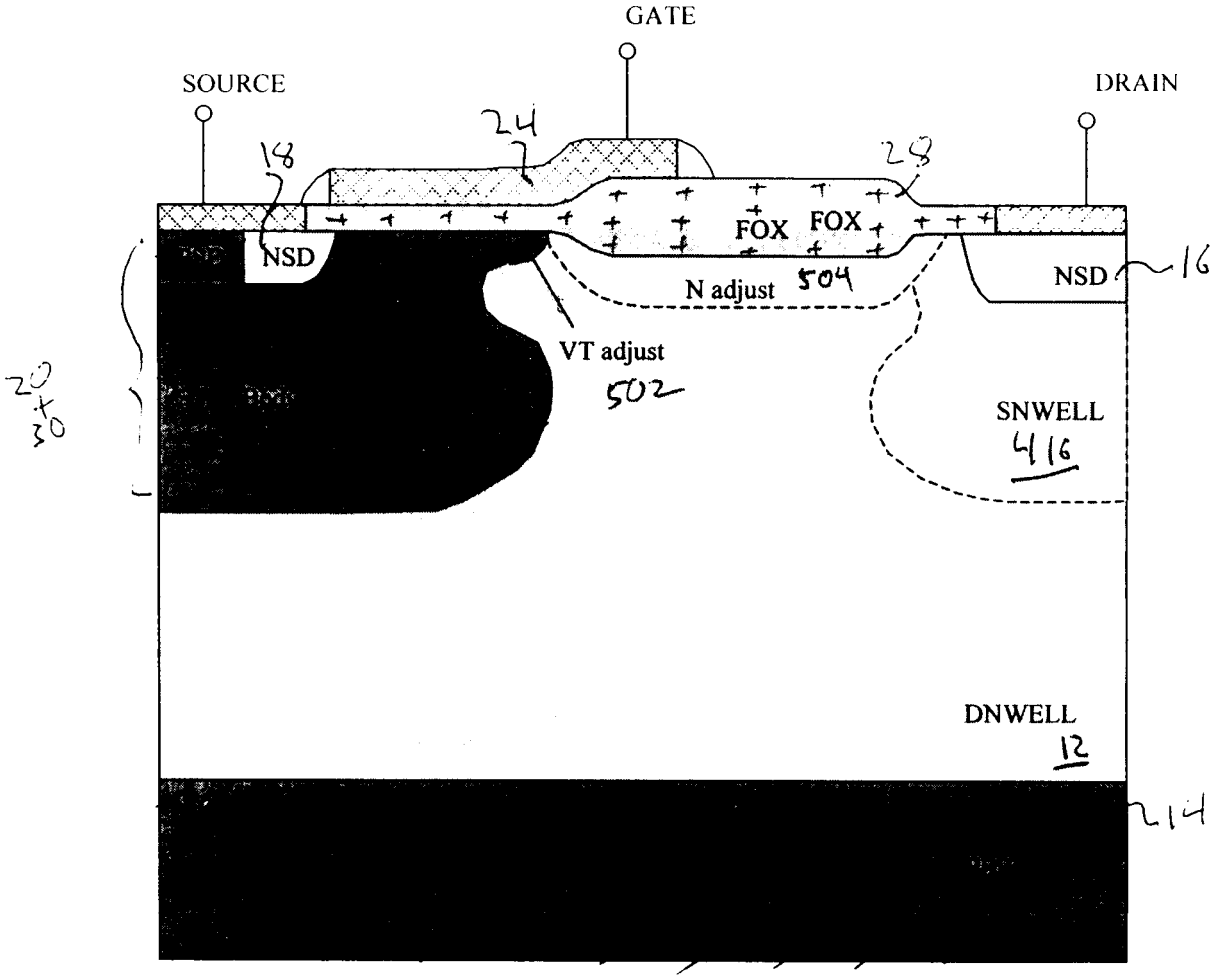


Fig. 5C